

# Producing Intelligent MMIC's with Multiple Optical I/O's for WDM Systems

- building on the silicon-on-gallium arsenide,  
and aligned pillar bonding techniques

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Singapore), Dr. Guiseppe Lullo, Hao Wang

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NEW MILLENIUM SERIES - overview of OE VLSI Research Program

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## Very Large Scale Optoelectronic Integration

### OBJECTIVES (our technology guidelines)

Electronics: VLSI densities and complexities  
State-of-the-art performance  
Standard design/layout/simulation tools

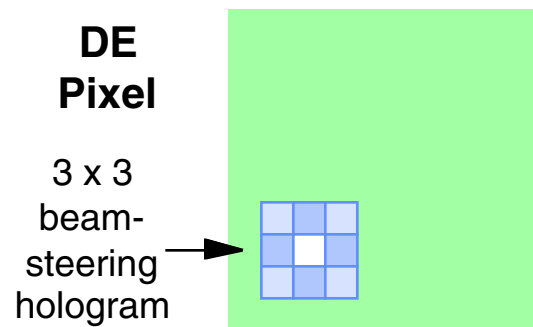
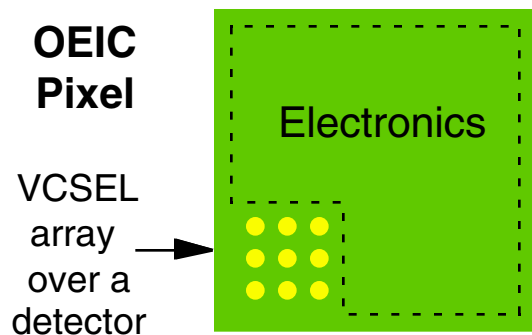
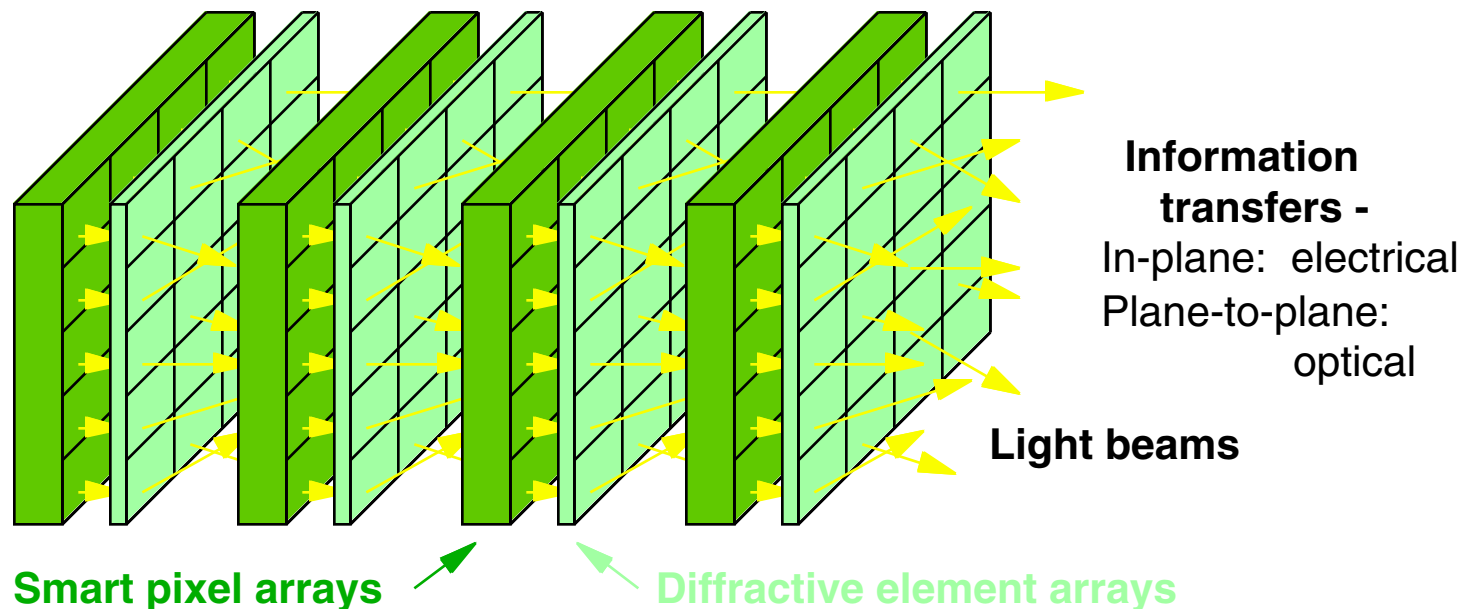
Optoelectronics: Unrestricted placement and quantities  
Uncompromised performance

Processing: Full-wafer processing  
Batch processing  
Standard, manufacturable processes

Our goal is to make high performance, very large scale OEICs....  
...economical and cost competitive,  
...available and accessible, and  
...useful and important.

## OEIC Technology Application: Smart Pixel Arrays

“computation, parallel processing of data and images, en/decryption”



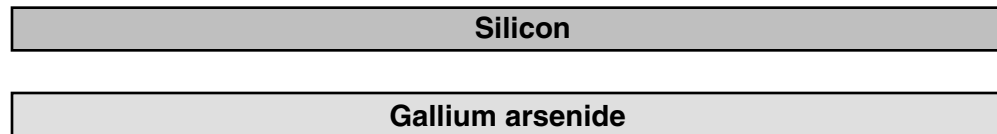
**Concept** (C. Warde):  
The plane-to-plane coupling pattern can be dynamically re-configured by selecting which VCSELs are illuminated.

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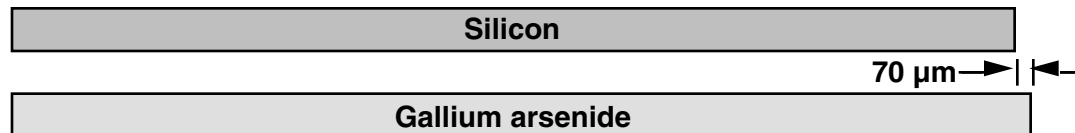
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## Understanding the Significance of the Difference in the Thermal Expansion Coefficients of Si and GaAs

**Wafers of Si and GaAs with identical diameters of 150 mm (6 in) \* at 15C:**



**If the temperature is raised 100C.....  
.....the GaAs wafer becomes 70  $\mu$ m larger than the Si wafer!**



**If the wafers are bonded, the stress is destructively large (i.e., they break).  
If the wafers are not bonded, any patterns on them are badly misaligned.**

**- and -**

**A change of 100C is small; 500C or greater is more typical.**

\* The industrial norm for Si is 200 mm (8 in), but you can find wafers as large as 300 mm (12 in).

## Very Large Scale Optoelectronic Integration

### APPROACH (meeting our objectives)

Exploit monolithic integration: economics of scale  
low parasitics, high reliability and yield  
high densities, small device footprints

Use a commercial IC foundation: highly developed technologies  
state-of-the-art performance  
fully developed models and tools for  
simulation, design and layout

Match thermal expansion coefficients: full-wafer processing  
reliable operation, long lifetimes

The key elements in our philosophy are...

- ...to reap all the benefits of monolithic integration
- ...to build on the investments of the Global IC industry
- ...to eliminate or accommodate thermal expansion mismatch

## The MIT processes for Monolithic Very Large Scale Optoelectronic Integration

### Epitaxy on Electronics (EoE)

- Concept:** Epitaxy on preprocessed electronics
- Features:** Full wafer, batch processing; monolithic integration; high planarity
- Done:** LED's on OPTOCHIP and other chips; SEEDs, RTDs, PINs, also
- Next:** VCSELs and IPSELs now being grown, integrated

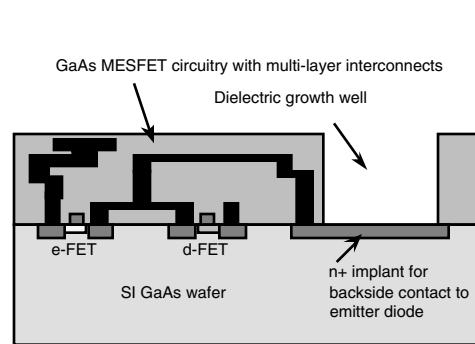
### Silicon on Gallium Arsenide (SonG)

- Concept:** Si-CMOS foundation for EoE and APB
- Features:** Thin Si to take the stress; unstressed optoelectronics for survival
- Done:** Preparation by bonding and thinning of 4" SonG wafers
- Next:** Epitaxy on SonG substrates; planarized CMOS bonding

### Aligned Pillar Bonding (APB)

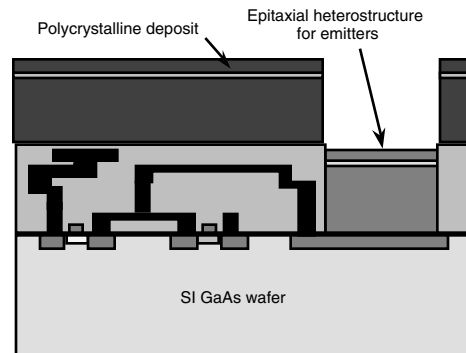
- Concept:** Aligned, Pd-bonding of heterostructures replacing direct epitaxy
- Features:** Optimal growth conditions, optimum substrate, all EoE features
- Done:** Pillars aligned and transferred; small features Pd-bonded
- Next:** More aligned bonding; VCSELs on OPTOCHIP; pin's on OEICs

## Epitaxy-on-Electronics (EoE)



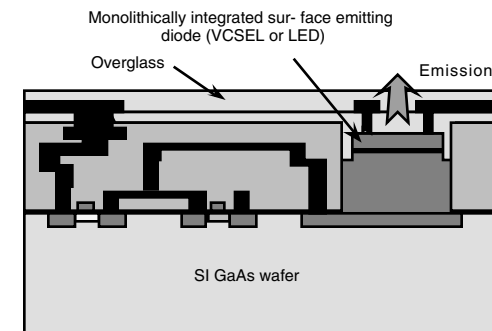
a.

Processed GaAs IC wafer as received from manufacturer



b.

After epitaxy and prior to removal of the polycrystalline deposit



c.

Optoelectronic device processing and interconnection completed

- Commercially processed GaAs electronics (circuitry custom-designed using standard layout and simulation tools; chips obtained through MOSIS)
- Monolithic processing, high surface planarity, no excessive overcoating of optoelectronic devices
- All processing compatible with full-wafer and batch processing (no lattice or thermal expansion coefficient mismatch)
- Conventional growth and fabrication of optoelectronic devices (growth temperatures must be under 475°C)

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## The Completed OPTOCHIP die

Free-space interconnect

M. W. Haney, GMU

Optical neural network

D. Psaltis, Caltech

Dynamic smart  
pixels

F. A. P. Tooley,  
McGill U.

Error-diffusion  
neural network

B. L. Shoop, USMA

Correlation network

C. W. Wilmsen, CSU

Remote sensing

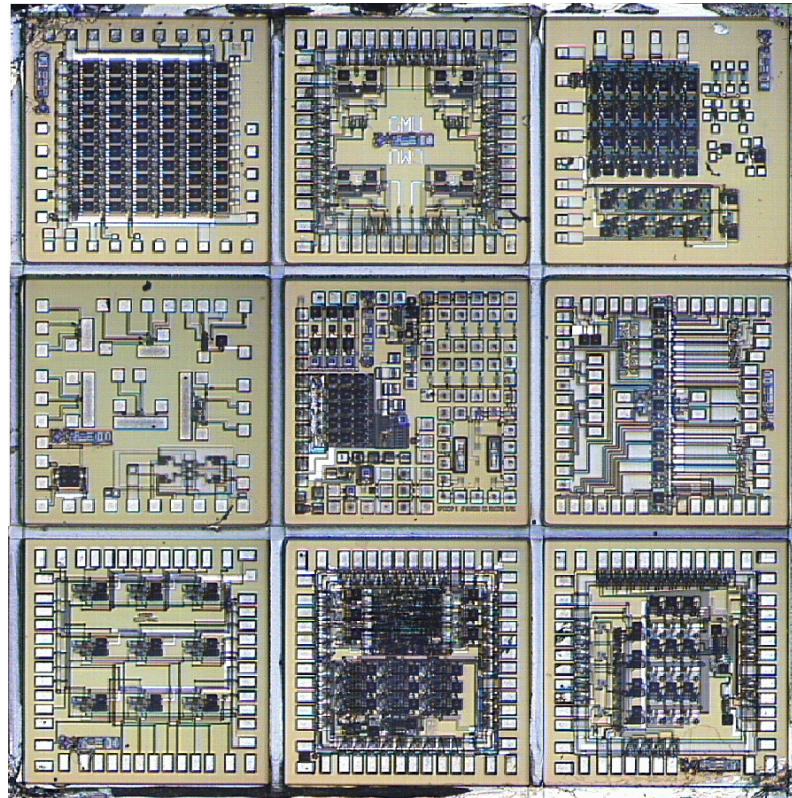
W. R. Babbitt,  
U. of Washington

Remote sensor  
interface

L. Cheng, TCU

Data-network interfaces

A. A. Sawchuk and T. M. Pinkston, USC



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**For many applications GaAs electronics is best, however...  
for memory and microprocessor intensive applications Si CMOS is best  
and for many people....Si CMOS is the only choice.**

## **How can we do EoE with Si electronics?**

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**Observation #1:** GaAs-on-Si has not worked because there is too much stress

**Observation #2:** Optoelectronic devices are intrinsically thick, but  
silicon MOSFETs are very thin.

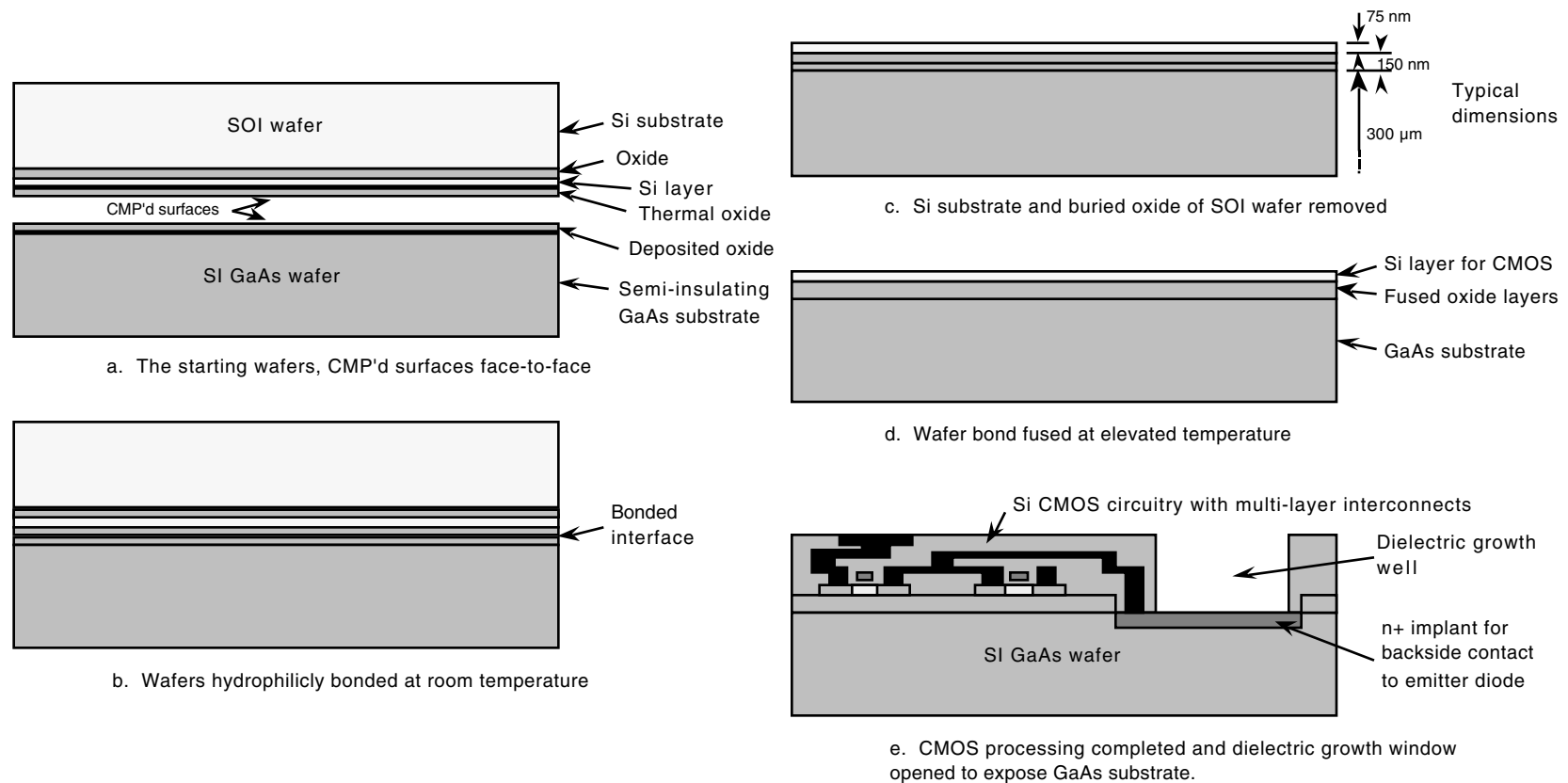
**Observation #3:** Thin materials can withstand large stresses,  
but thick materials can not.

**The answer:** Thin silicon and thick GaAs can work together in the  
spirit of SOI, and especially SOS (Si-on-sapphire),

## **....Silicon-on-Gallium Arsenide (SonG)**

**Note:** The clearest proof that this can work is SOS (Si-on-sapphire).  
(The thermal expansion coefficient of GaAs equals that of sapphire.)

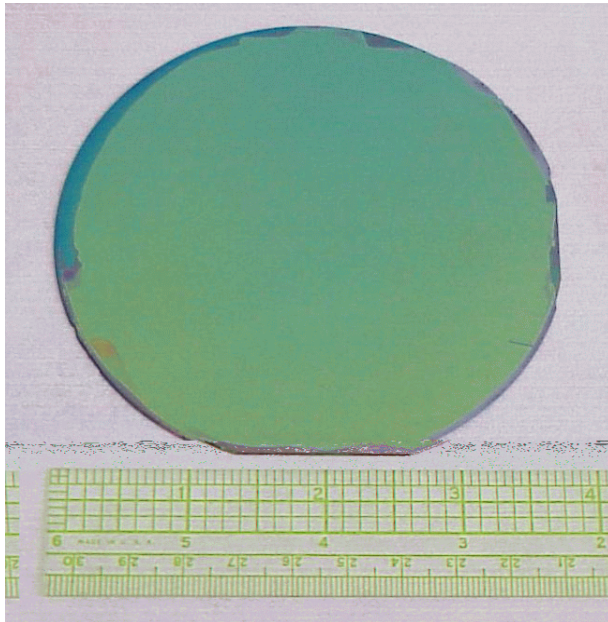
# The MIT Si-on-GaAs Process for Monolithic Heterogeneous Integration of GaAs-based Optoelectronics with Silicon CMOS



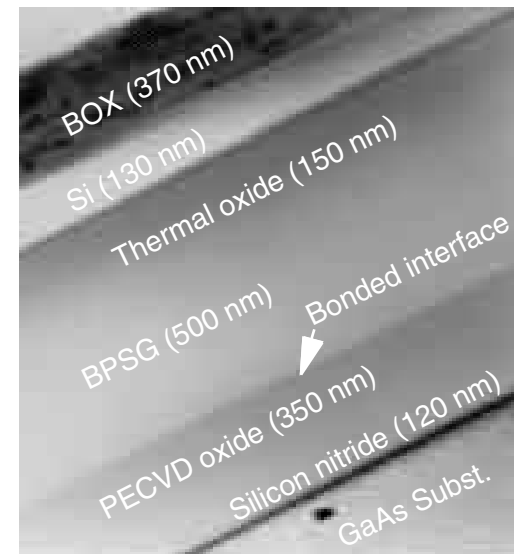
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## Silicon-on-Gallium Arsenide Wafers - created by bonding and thinning



Four inch SonG wafer



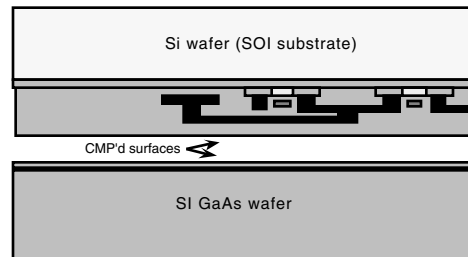
Cross-sectional TEM

- Refs: J. M. London, A. H. Loomis, J. F. Ahadian, and C. G. Fonstad, Jr., "Preparation of silicon-on-gallium arsenide wafers for monolithic optoelectronic integration," IEEE Photonics Tech. Lett. 11 (1999) 958-960,  
J. M. London, P. A. Postigo, and C. G. Fonstad, Jr., "Quantum well heterostructures grown by molecular beam epitaxy on silicon-on-gallium arsenide substrates," Appl. Phys. Lett. 75 (1999) 3452-3454.

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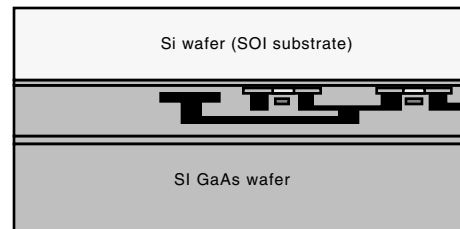
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## Silicon-on-GaAs (SonG) providing CMOS substrates for EoE and APB



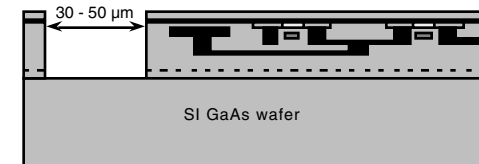
a.

The bulk GaAs wafer and the processed SOI CMOS wafer placed face to face prior to bonding.



b.

After hydrophilic room temperature bonding and prior to removal of the CMOS wafer substrate and high temperature fusion of the bond.



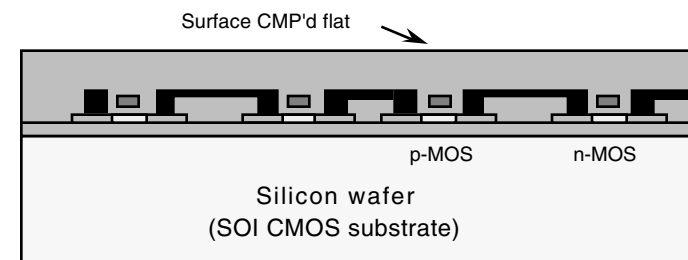
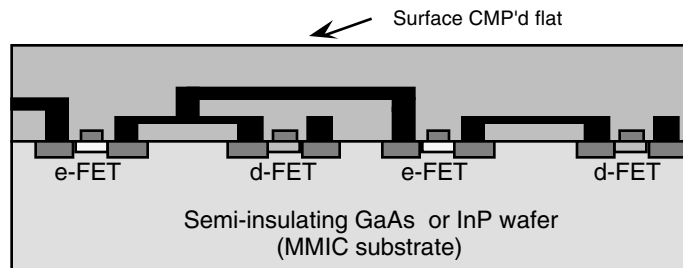
c.

After substrate removal, bond fusion, and preparation of windows for EoE or APB processing.

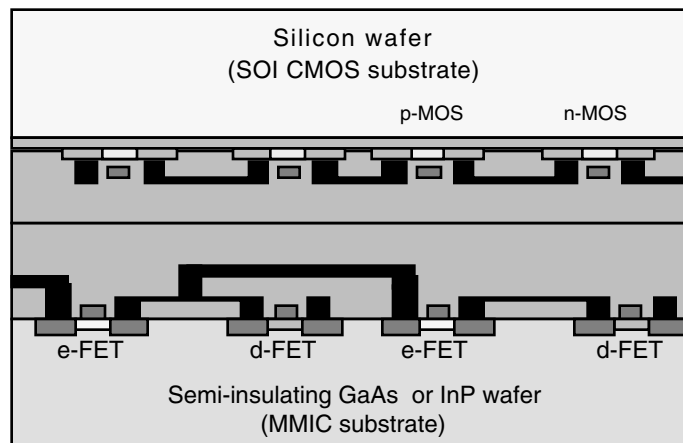
- GaAs substrate provided for inherently thick, strain-sensitive optoelectronic devices
- Silicon made no thicker than necessary to withstand stresses arising during high temperature processing steps
- Building on advances in MEMS, SOI, CMOS, and EoE
- Monolithic integration, full-wafer processing

## Integrating Si-CMOS Intelligence and Memory on III-V MMICs using the SonG Process

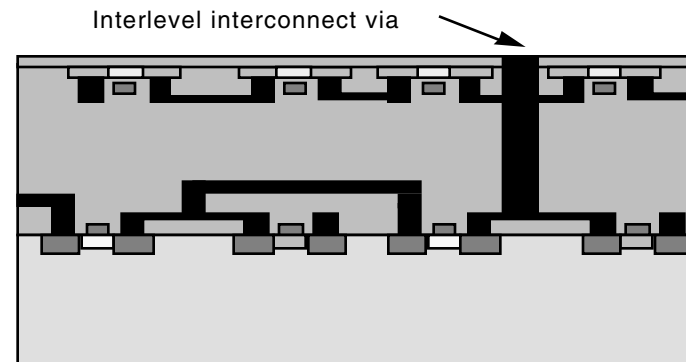
heterogeneous integration for microwave and WDM applications



a. Processed and planarized MMIC and SOI CMOS wafers prior to bonding. Note that the MMIC wafer could be either InP or GaAs based and could use MESFETS, HEMTs, or HBTs. In the example illustrated GaAs MESFETs are pictured.



b. After low-temperature bonding of the MMIC and CMOS wafers, and prior to the removal of the substrate of the CMOS wafer.



c. After removal of the SOI CMOS wafer substrate, strengthening of the bond, and formation of the interlevel interconnects.

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## - Aligned Pillar Bonding -

**EoE has limitations** (whether on GaAs or SonG):

- \* The epitaxy conditions are not always optimal
- \* The substrate choice is not totally free; may not be optimal

Thus we ask:

**"How can we get the device heterostructures in dielectric windows on ICs other than through epitaxy?"**

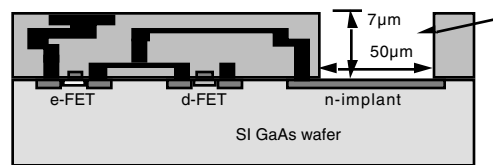
and the obvious response is: **"Wafer bonding"**

Specifically...aligning and bonding pillars etched on a heterostructure wafer in the dielectric windows on a processed integrated circuit wafer

### **...ALIGNED PILLAR BONDING (APB)**

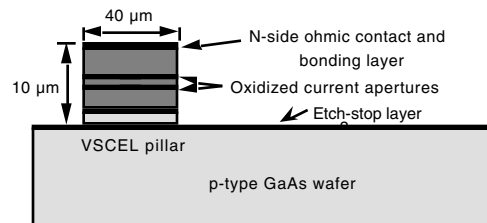
- Notes:**
- \* The bonding temperature will be limited by the electronics.
  - \* We must still match TECs, or we must bond at R.T. sufficiently to remove the substrate.
  - \* The bonding must be uniform and complete on a very fine scale, and over the entire wafer.
  - \* APB can be done on silicon-on-sapphire (SOS) wafers also!

## Aligned Pillar Bonding (APB)



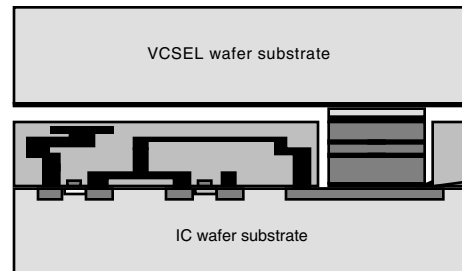
a.

The processed IC wafer as received from the manufacturer



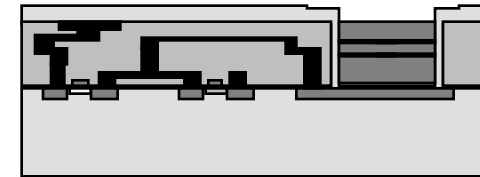
b.

The p-side down VCSEL wafer with pillars etched to match the windows on the IC wafer



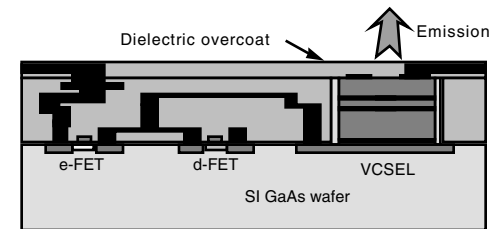
c.

After alignment and bonding of the VCSEL and IC wafers (note that only one well and pillar are shown, whereas many thousands are integrated simultaneously in the processing of full wafers)



d.

After removal of the substrate of the VCSEL wafer leaving VCSEL heterostructures bonded in windows. Further processing proceeds as in the EoE process.



e.

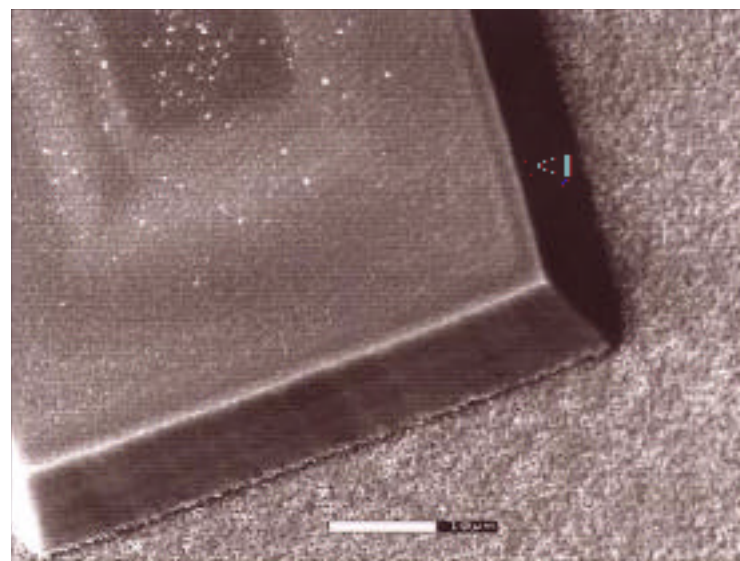
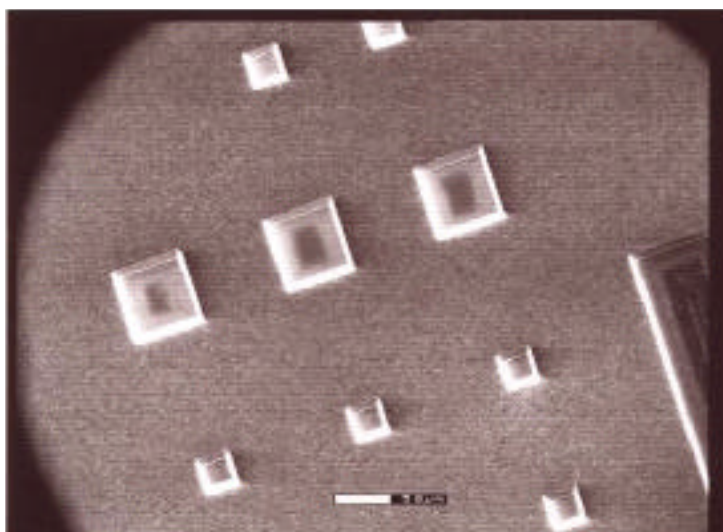
Device processing, integration complete

- Optoelectronic heterostructures can be grown under optimal conditions on optimum substrates; bonded to GaAs or SOS
- All features of EoE process retained
- Near-room temperature bonding would enable integration of InP-based optoelectronics and silicon-based electronics



# **Aligned Pillar Bonding**

## GaAlAs Heterostructure LED Pillars bonded on GaAs

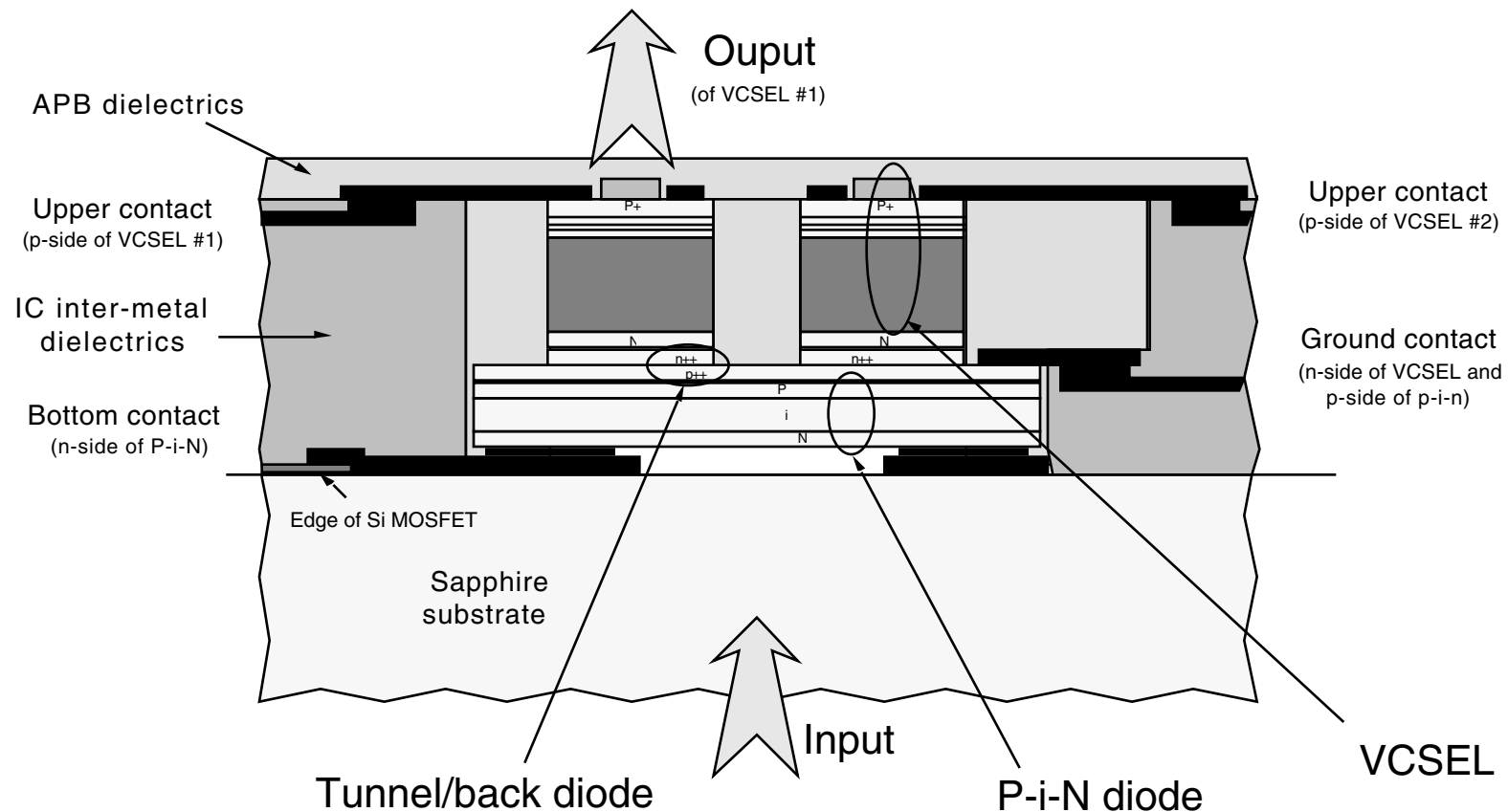


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## APB-integrated P-i-N Diode/VCSEL Stack

- array of top-emitting VCSELs over a bottom-input photodetector
  - illustrated on a Silicon-on-Sapphire integrated circuit

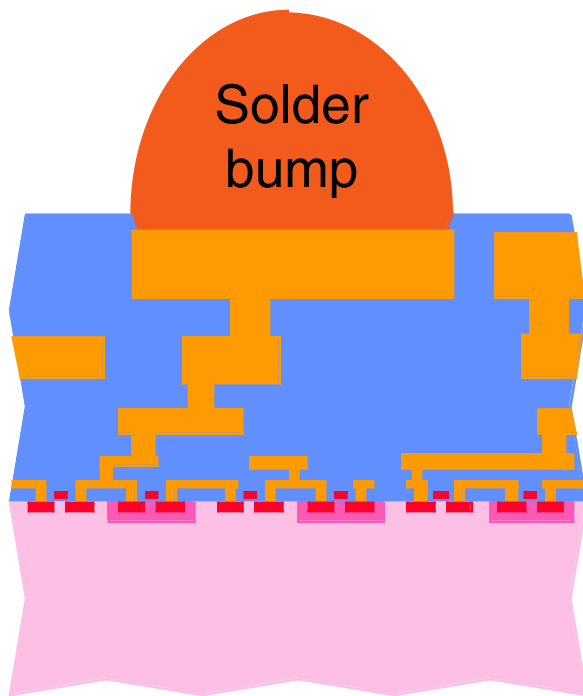


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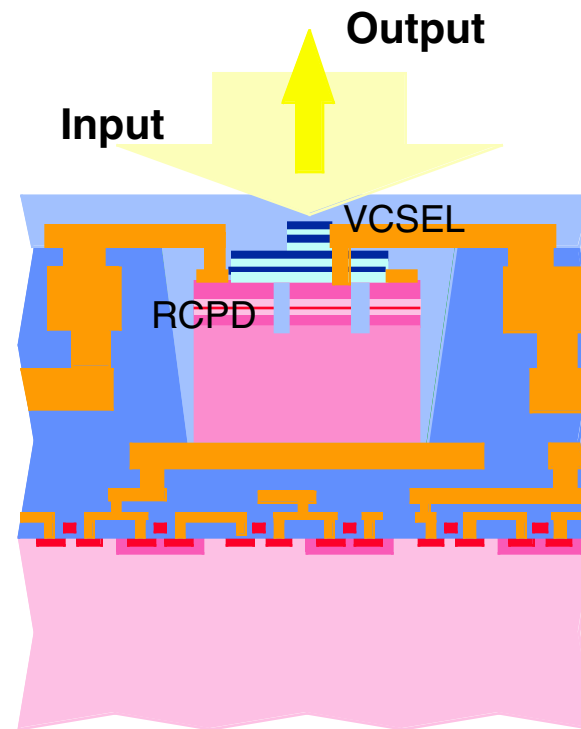
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# The Optical Solder Bump Concept

- the solution to doing chip-to-chip optical signal transfer on MCMs....  
....make 95% of the solder bumps on a chip are optical bumps!



**A traditional solder bump**



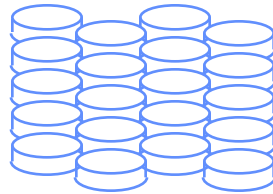
**An optical solder bump**

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## Optical solder bump assembly using bilateral pills

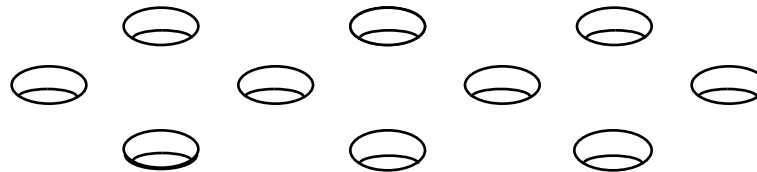
Device pills  
patterned  
through  
epilayers.



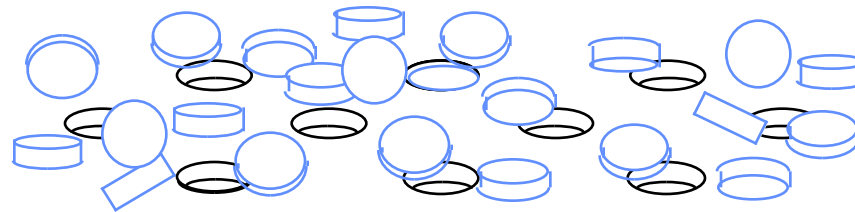
Device pills  
etched free  
of substrate.



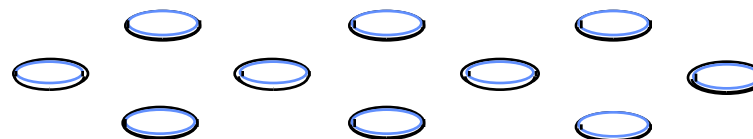
Dielectric device  
recesses etched  
into CMOS wafer.



Device pills tumbled  
over recesses on  
CMOS wafer.



Device pills in place  
filling all recesses on  
CMOS wafer.



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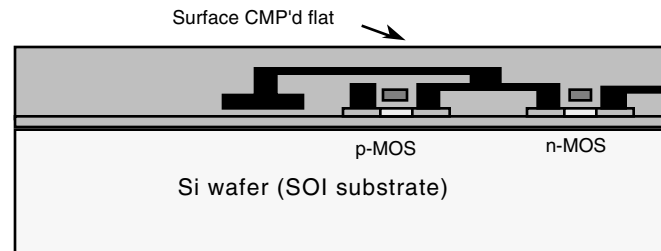
Looking further ahead:

## Monolithic Integration of CMOS, DCFL, and VCSELs

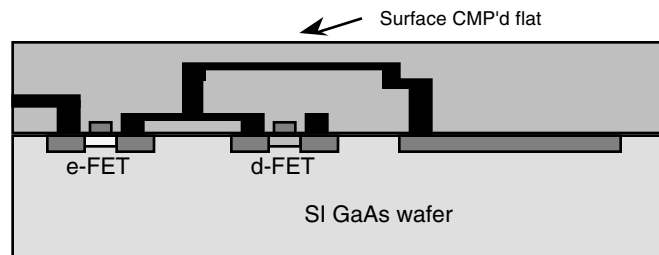
DCFL: multi-Gbps signal processing

CMOS: memory,  $\mu$ -processors

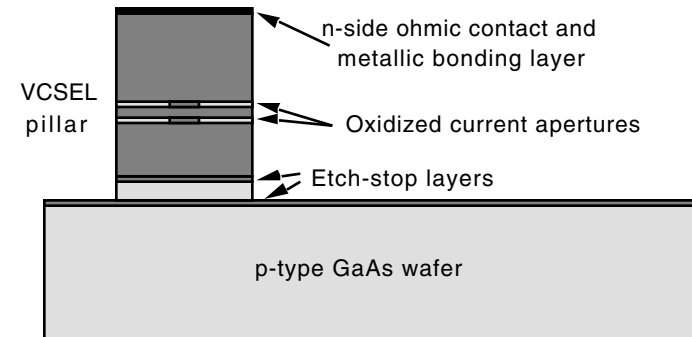
VCSELs: optical data transfer



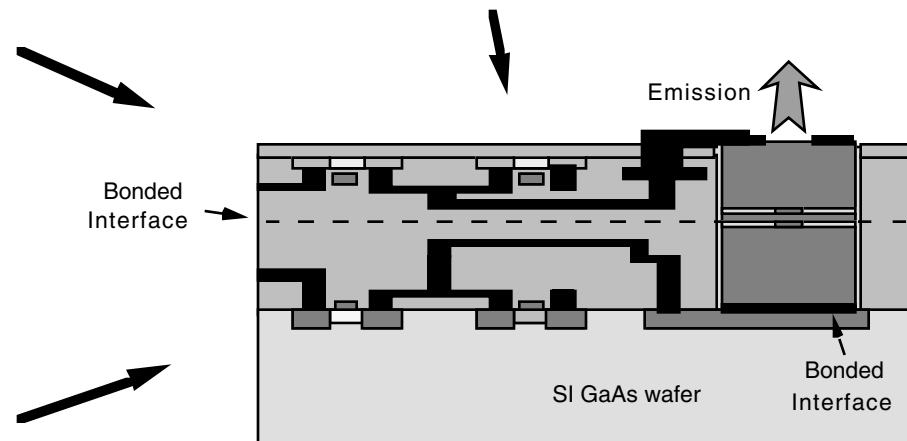
SOI CMOS wafer (planarized)



GaAs DCFL wafer (planarized)



VCSEL wafer (partially processed)



Note: Alternatively VCSEL layers can be EoE-grown directly into the device window on the bonded GaAs-CMOS wafer pair.